An 8–15 GHz GaAs Monolithic Frequency Converter

RAVI RAMACHANDRAN, SANJAY B. MOGHE, MEMBER, IEEE, GARY LIZAMA, PANG HO, SENIOR MEMBER, IEEE, AND ALLEN F. PODELL, SENIOR MEMBER, IEEE

Abstract **—An MMIC frequency converter with an RF bandwidth of 8–15 GHz and an IF bandwidth of 1.5 GHz has been designed and built. The MMIC chip has 15 dB conversion gain and includes a two-stage RF amplifier, a two-stage LO buffer amplifier, a double-balanced mixer, and a three-stage IF amplifier. This high level of integration is realized on a small—48×96 mil—area, resulting in good RF yields. The circuit employs a push–pull configuration to eliminate the need for via holes (low-inductance grounds) and facilitate a compact layout.**

I. Introduction

MICROWAVE FREQUENCY converters are widely used in commercial and military communication systems. At present, these are primarily hybrid MIC subsystems that integrate RF amplifiers, mixers, and IF amplifiers. Each of these components has to be built, tested, and tuned separately and then interconnected using short cable lengths or microstrip lines. The cost of the individual components as well as the additional tuning necessary to reduce the effect of interconnection mismatches makes this an expensive system. The size and the weight of such a product are substantial. MMIC converters, therefore, provide great advantages of cost, size, weight, and reliability over their MIC counterparts. However, few broad-band MMIC converters have been built to date because of the difficulties involved in realizing broad-band amplifiers and mixers at K_u-band frequencies and combining them with IF amplifiers within a single chip of reasonable size. A previously reported MMIC frequency converter [1] showed excellent performance across the 3.7–4.2 GHz band. The novel transformer-coupled circuits used resulted in high levels of integration and compact size. At higher frequencies, it is harder to realize such complex subsystems on a chip due to difficulties in modeling interactions between the various components of the system, grounding problems, and parasitic effects.

Our work, reported in this paper, shows that broad-band lossy match amplifiers using lumped-element matching networks, and transformer-coupled diode mixers operating at K_u-band frequencies can be integrated, along with IF amplifiers, to obtain a complete high-performance receiver IC. This K_u-band down-converter has one of the highest levels of integration reported to date in high-frequency analog MMIC's. It incorporates 20 FET's, 35 spiral inductors, 40 resistors, and 26 MIM capacitors on a single chip.

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The authors are with Pacific Monolithics, Inc., Sunnyvale, CA 94086-4512

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II. MMIC Frequency Converter Circuit Description

The cell library approach, reported earlier [2], was used in developing this subsystem MMIC. In this approach, each component required for a system is first developed and fully characterized individually. Then these different cells are integrated within a single MMIC. The individual cells are designed to have low input and output VSWR to minimize unpredictable interactions between different cells. If this is not possible, at least one of the interconnecting cells is designed to have low VSWR so that the overall performance can be predicted easily. Because of the extremely short interconnection lengths involved, the resultant parasitics and VSWR degradation are kept to a minimum, resulting in a predictable, high-performance IC.

Fig. 1 is the block diagram of the fully integrated receiver chip. The chip consists of a two-stage, broad-band RF amplifier, a two-stage LO buffer amplifier, a double-balanced mixer, and a three-stage IF amplifier. In addition, all the matching, biasing, blocking and bypass circuits are included on the chip. The amplifiers compensate for the mixer conversion loss, provide buffering to the mixer, and increase the isolation from port to port.

In the following paragraphs we shall describe the technical approach used in designing the converter and the individual circuits (cells) that form the building blocks of the IC. Measured results for these individual cells, as well as the complete converter, will also be presented. Finally, the main factors that affect the performance of the converter will be summarized.

III. Push–Pull Approach

The push–pull circuit technique has been used extensively for low-frequency amplifiers. Recently, its use at microwave frequencies has been successfully demonstrated [3], [4]. In this chip, the push–pull configuration has been used throughout in the design of the individual component cells, for several reasons. One of the features of the push–pull technique is the presence of a virtual ground between the push–pull amplifiers. This eliminates the need for critical RF grounding by means of via holes and allows

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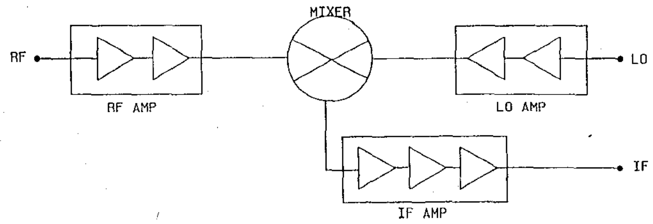

Fig. 1. Block diagram of MMIC down-converter.

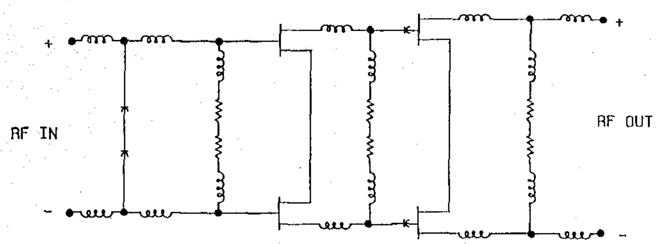

Fig. 2. Functional schematic of RF amplifier.

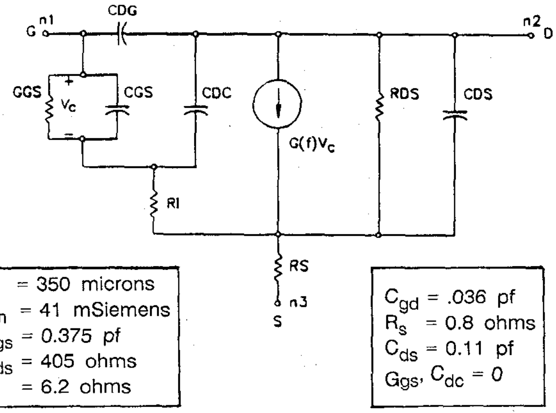

Fig. 3. FET model used in RF amplifier design.

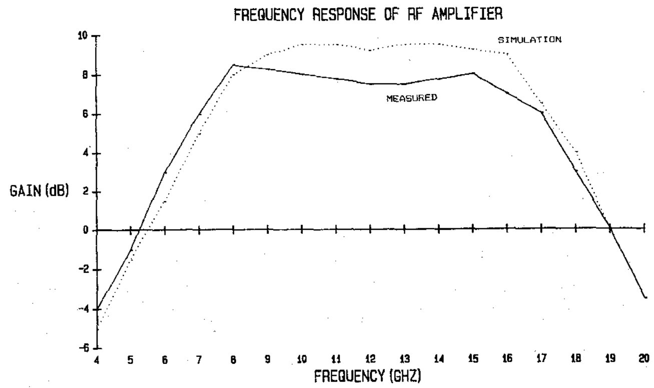

Fig. 4. Gain response of RF amplifier.

close packing of the various components. The yield is also increased since via holes are no longer necessary during wafer processing and the foundry process is less complex. These factors are of special significance for complex subsystem IC's where the large chip size tends to reduce the yield.

Even though push–pull circuits tend to be larger and more complex and require baluns at the input and output, they are capable of higher output power and can directly drive balanced loads (for example, a diode quad mixer). Also, in a complex subsystem composed of many balanced circuits, the internal connections within the system can be made directly and baluns are required only at the input and output ports.

IV. RF Amplifier Design

Fig. 2 is the functional schematic of the RF amplifier. The RF amplifier is a two-stage, push–pull circuit designed to operate over the 8–16 GHz band. The lossy match technique for broad-band amplifiers [5], [6], is used to obtain flat gain response over the octave bandwidth, along with low input and output VSWR. Only lumped elements are used in the matching networks, so that the circuit size is minimized. Computer modeling programs have been used to design the spiral inductors. The amplifier was limited to two stages to minimize dc power consumption.

Fig. 3 shows the FET model used in the design of the amplifier. The amplifier response was simulated using Touchstone^{TM}. The spiral inductors were modeled as lumped elements with parasitic resistors and capacitors added. The computer programs that were used to design the spiral inductors also calculate the series parasitic resistance associated with the inductor, and these are included in the model during circuit simulation. A typical inductor value is 1.5 nH with a series resistance of 5 Ω. This series resistance varies with frequency and the variation is accounted for during RF simulation. The parasitic capacitances were derived from measured data. These models have been used extensively and they have predicted the RF performance with good accuracy. Fig. 4 shows the simulated and measured gain responses of the RF amplifier. The close agreement between the two confirms the validity of the active and passive element models used. The RF amplifier provides 8 ± 1 dB gain over the 8–16 GHz band while drawing 40 mA from an 8-V supply. The input and output VSWR's are less than 2:1.

The LO buffer amplifier is similar in design and is capable of delivering the required 13 dBm drive power for the mixer. It also uses an 8-V supply and draws 50 mA.

V. Double-Balanced Mixer and IF Amplifier Design

The successful implementation of an MMIC converter requires the design of a wide-band mixer, with low conversion loss, that can be realized in a small-size monolithic form. The mixer used here is a planar version of the double-balanced, transformer-coupled, diode mixer widely used at lower frequencies; its schematic is shown in Fig. 5. It occupies very little area, and consumes no power since it is a passive circuit. Planar transformers are used to couple signals into a diode quad. The diode quad consists of four 1-μm GaAs interdigitated diodes, with a periphery of 72 μm each. These are N+ diodes, and therefore have low series parasitic resistance. The spiral transformers consist of closely coupled planar spiral inductors. The inductance

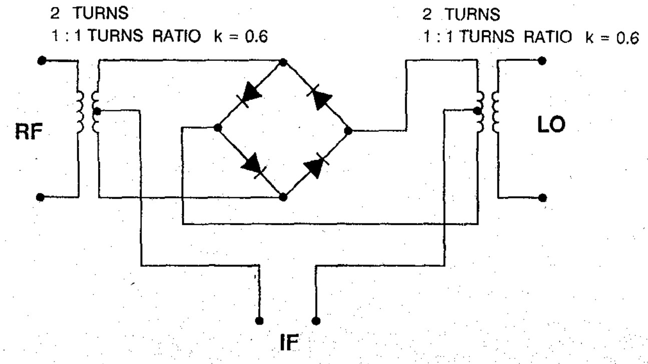

Fig. 5. Schematic of double-balanced diode mixer.

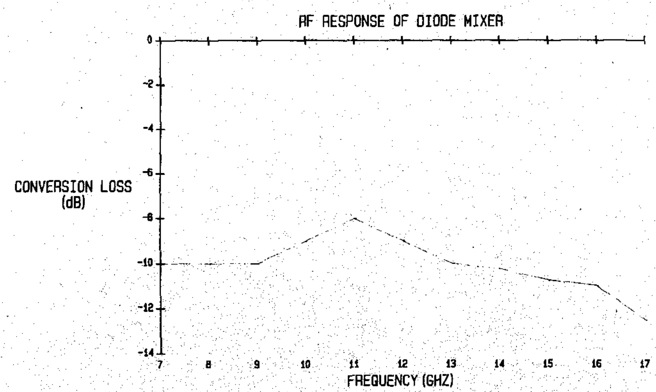

Fig. 6. Measured RF response of monolithic diode mixer.

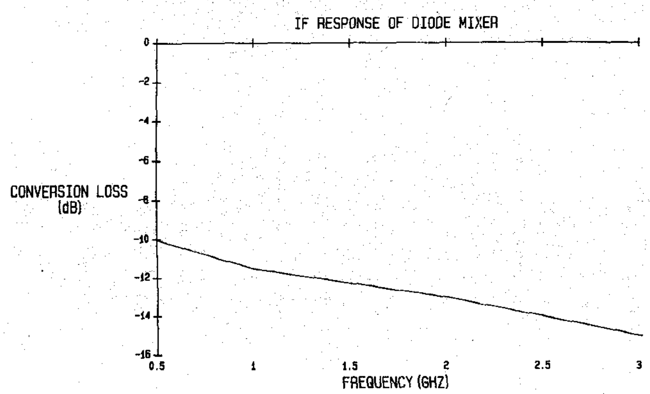

Fig. 7. Measured IF response of monolithic diode mixer.

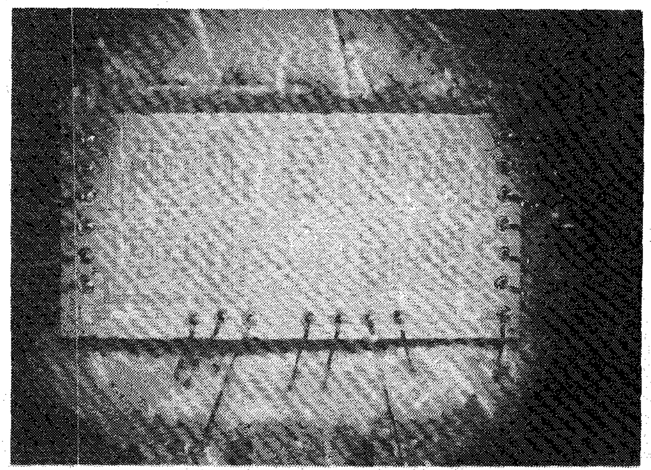

Fig. 8. Photograph of MMIC down-converter chip.

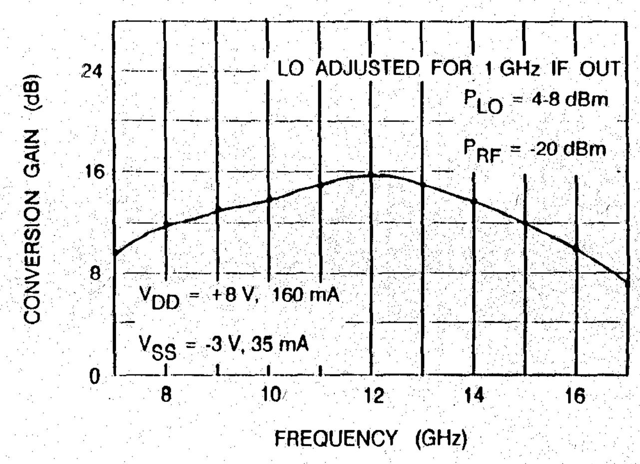

Fig. 9. Conversion gain versus RF frequency.

of these coils and their coupling factor are computed using a bifilar version of the inductor modeling program that was used for the spiral inductors. While the coupling factors for planar spiral inductors are considerably less than unity, the results obtained herein prove they are sufficient for reasonably broad bandwidths. Fig. 6 shows the RF response of this mixer measured separately. The roll-off at low frequencies is caused by the short-circuiting effect of the spiral transformer, whereas the high-end roll-off can be attributed to increasing losses in the high-impedance lines. Fig. 7 shows the measured IF response of the mixer. The increased conversion loss for frequencies beyond 1 GHz is caused by the self-inductance of the transformer windings and the low coupling factor between the secondary turns.

The IF amplifier uses two common source stages and one source follower stage to deliver approximately 15 dB of gain over the 0.1–2 GHz band. The two common source stages provide the gain, and the source follower stage is used to obtain a good output match. It is also a compact push–pull amplifier designed for easy integration with the mixer, occupying only a 24×24 mil area. Fig. 8 is a photograph of the complete converter chip.

VI. RF Performance

RF measurements were performed on the MMIC converter with baluns at the RF and LO ports. These were quarter-wavelength coplanar MIC baluns that cover over an octave bandwidth. Even though the IF output was also push–pull, one of the ports was terminated for ease of measurement, and single-ended data were recorded. For determining the RF response of the converter, an IF frequency of 1 GHz was chosen, and the LO frequency adjusted suitably as the RF input was varied from 7 to 15 GHz. The resultant conversion gain is plotted in Fig. 9. The gain varies from 12 to 16 dB in the 8–15 GHz band, with a peak conversion gain of 16 dB at 12 GHz. The LO power applied was less than 8 dBm in all cases, while the RF level was maintained at −20 dBm. Even though the

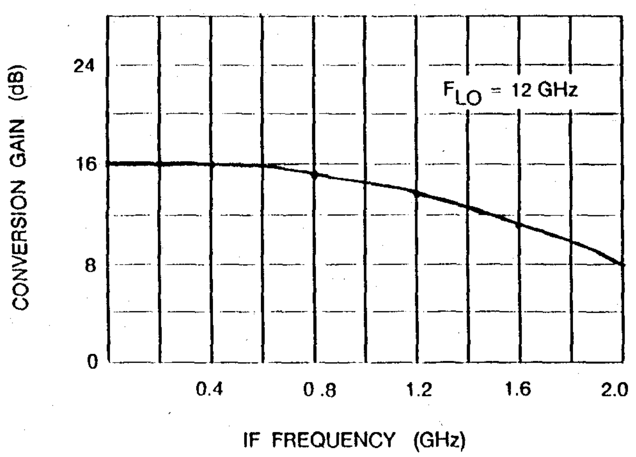

Fig. 10. IF response of MMIC converter.

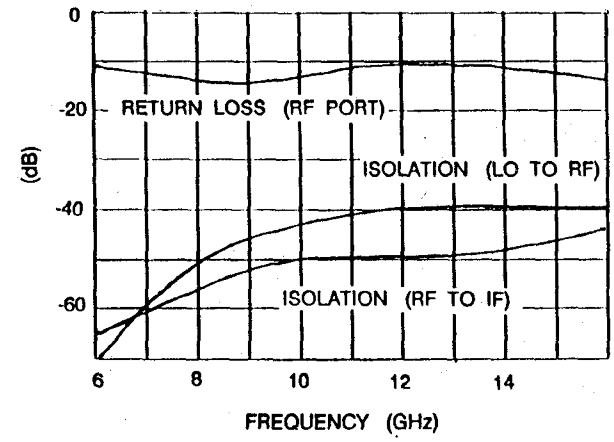

Fig. 12. Return loss and isolation.

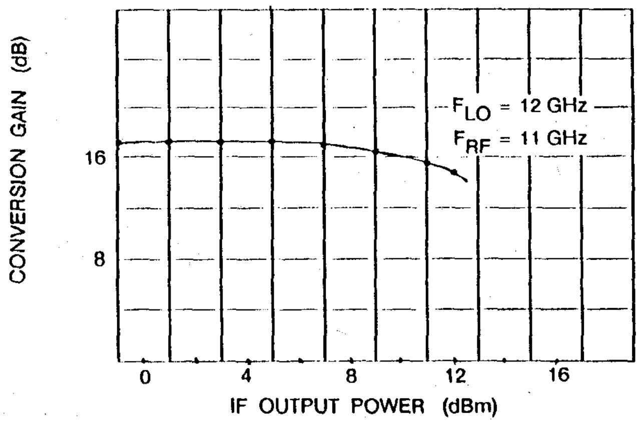

Fig. 11. Conversion gain versus IF output power.

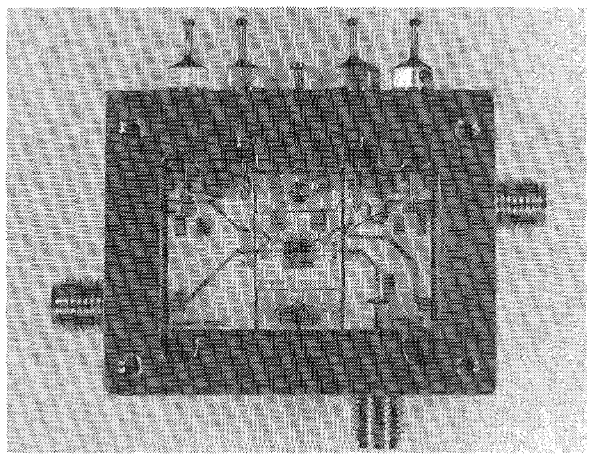

Fig. 13. MMIC down-converter assembled in housing.

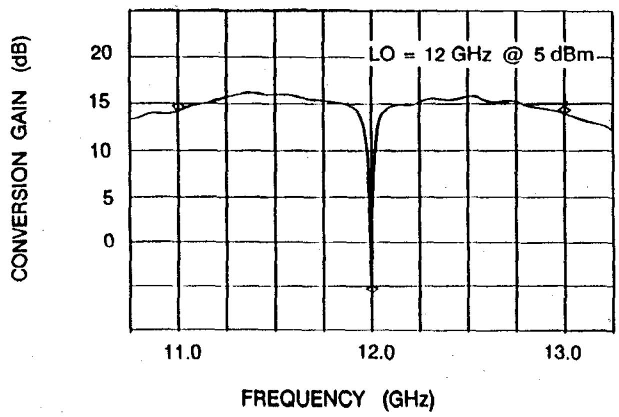

Fig. 14. Typical response of MMIC converter assembled in housing.

RF amplifier gain was about 2 dB less than the simulation, the IF amplifier gain was about 3 dB higher than predicted, so that the overall conversion gain was very close to the predicted value of 15 dB at midband. The IF response of the converter is plotted in Fig. 10, with the LO frequency held constant at 12 GHz. The IF response indicates an IF bandwidth of 1.5 GHz for a conversion-gain flatness within ± 2 dB. The overall response of the converter is determined by the individual responses of the mixer and the RF and IF amplifiers. It should be noted that the mixer limits both the RF and the IF bandwidths, whereas the RF and IF amplifiers only affect their respective bandwidths. The use of a distributed amplifier as well as a transformerless mixer can result in extremly broad-band converters.

Fig. 11 is a graph of the conversion gain as a function of the IF output power. The 1-dB compression point for the converter is approximately 10 dBm. The return loss and isolation measured on the chip are plotted in Fig. 12. The VSWR at the RF and LO ports is less than 2:1. Use of the double-balanced mixer and buffer amplifiers also results in over 40 dB isolation from port to port. Fig. 13 is a photograph of the MMIC chip assembled in a housing along with thin-film MIC support circuitry. The typical conversion gain of the assembled system is plotted in Fig. 14. The conversion gain is approximately 15 dB in the 11–13 GHz band, and closely matches the chip in performance. The yield across the wafer for this converter IC was over 60 percent, and the yield from wafer to wafer did not vary much for the several wafers that were tested.

VII. Conclusions

It has been demonstrated that, using a cell-library approach, a high level of integration is possible in GaAs MMIC's. Several analog functions can be combined on a single chip to build high-performance subsystem IC's at low cost. An 8–15 GHz GaAs monolithic frequency converter IC has been developed which exhibits repeatable and predictable performance with high yield.

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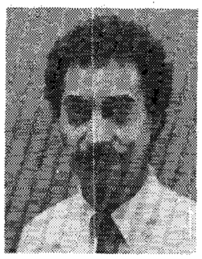
Ravi Ramachandran was born in Madras, India, on July 27, 1958. He received the B.Tech degree in electrical engineering from the Indian Institute of Technology in Madras in 1980, and the M.S.E.E. from Rensselaer Polytechnic Institute, Troy, NY, in 1981.

From 1982 to 1984 he was with the Narda Microwave Corporation, designing and developing dielectric resonator oscillators and hybrid MIC subsystems. From 1984 to 1986 he was part of the GaAs MMIC design team at Avantek, involved in developing medium-power and nonlinear MMIC circuits. He is currently a senior engineer at Pacific Monolithics, working on the development of wide-band GaAs MMIC's.

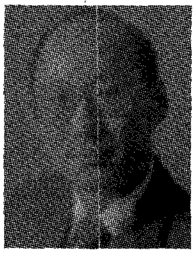
Sanjay B. Moghe (S'75–M'80) received the B.S. degree in physics from Delhi University, India, in 1972, the M.S. degree from the University of Louisville, KY, in 1976, and the M.S. and Ph.D. degrees in electrical engineering from Rensselaer Polytechnic Institute, Troy, NY, in 1978 and 1982, respectively.

From 1976 to 1979 he worked as a research assistant at Rensselaer Polytechnic Institute and studied the effects of radiation on GaAs MESFET's. From 1979 to 1982 he worked at the Raytheon Company, developing hybrid low-noise and power GaAs MESFET amplifiers. In 1982 he moved to the R&D Laboratory at Avantek, where he was responsible for the development of GaAs monolithic microwave integrated circuits. At Avantek he developed some of the first high-performance low-noise and power MMIC amplifier circuits that were manufactured in high volume. From 1983 to 1985 he was the manager of the MMIC design group. In 1985, he joined the staff of Pacific Monolithics as Manager of MMIC engineering. Presently, he directs a team of GaAs MMIC designers developing analog and digital GaAs monolithic products, including amplifiers, switches, oscillators, phase shifters, mixers, dividers, receivers, and subsystems using these basic blocks.

Dr. Moghe has authored 25 technical papers on low-noise and power amplifiers, MMIC receivers and oscillators, mixers, MIC and MMIC design techniques, FET characterization, and radiation effects in GaAs MESFET's. He is a member of Sigma Xi and of the Technical Program Committee of the International GaAs IC Symposium.



Gary Lizama was born in Kingston, Jamaica, on August 12, 1962. He received the B.S. degree in electronics engineering from Santa Clara University in 1985. He is currently working at Pacific Monolithics in the areas of MMIC switches and attenuators and subsystem engineering.



Pang Ho (M'76–SM'81) received the B.S.E.E. degree from National Taiwan University, Taiwan, Republic of China, in 1967, the M.S.E.E. degree from Princeton University in 1969, and the Ph.D. degree from Rutgers, the State University of New Jersey, in 1975. In 1985, Dr. Ho joined Pacific Monolithics as Vice President of Engineering. His effort is focused on the development of microwave components and subsystems using monolithic microwave GaAs IC technology.

Dr. Ho has published over 35 technical papers on semiconductor devices, microwave integrated circuits, and microwave communication systems. He holds 11 U.S. and European patents. He is past chapter chairman of the IEEE Microwave Theory and Techniques Society. In 1983 he received the IR-100 award from Industrial Research and Development for the development of a high-speed switch matrix system for NASA.

From 1969 to 1976 he worked for the RCA Solid State Division, and the David Sarnoff Research Center. He worked on a solid-state transceiver module for *L*- and *S*-band phased-array radar, device processing and circuit design of a microwave bipolar power transistor, high-power p-i-n diode, the IMPATT and TRAPATT diode. From 1976 to 1983, he was with the Ford Aerospace and Communications Corporation. As Manager of Advanced Communication Systems Engineering, he was responsible for the development and pilot production of 14-GHz receivers for the INTELSAT-V program. He developed a space-qualified *C*-band 10-W FET power amplifier, a K_u-band low-noise FET amplifier, and 20×20 microwave switch matrix. From 1983 to 1985, he was President of Geotech Communications, Inc., a manufacturer of satellite TV systems for the home and commercial use.

Allen F. Podell (S'60–M'61–SM'77) holds a B.S. engineering physics degree from Cornell University. He is presently Chairman of the Board, Senior Vice President, and Director of Technology Development at Pacific Monolithics of Sunnyvale, CA, a company he cofounded in 1984.

In 1960 he cofounded Anzac Electronics, now a division of the Adams Russell Microwave Company. He developed Anzac's unique line of ultra-broad-band RF couplers, mixers, hybrids, combiners, and switches, and directed the company's growth from start-up to productivity. From 1968 to 1970 he was Corporate Director of Product Innovation at Adams Russell. His responsibility covered RF engineering development throughout the company. He developed broad-band hybrids, transformers, phase shifters, power amplifiers, mixers, and special-purpose test equipment. From 1970 to 1972 he specialized in extremely broad-band components and matching networks at Stanford Research Institute, as Senior Research Engineer. From 1972 to 1977, as R&D Manager at Hewlett Packard, he evaluated and recommended technology strategies for new products and participated in the design of H–P's first complex GaAs IC's, including 3.5-GHz operational amplifiers, digital word generators, digital shift registers, and 2–18-GHz oscillators. From 1977 to 1978 he was Chief Engineer at Varian Associates at their Solid State Microwave Division. He developed a five-year plan aimed at making the division profitable, developed new product strategy, and defined R&D projects. In 1978 he founded Allen F. Podell & Associates, providing consultation on the design of microwave amplifiers, sources, and both digital and analog GaAs IC's, as well as electromechanical design.